UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,716	03/15/2004	Shiro Dosho	60188-803	8987

20277 7590 05/12/2005

MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

EXAMINER	
LE, DINH THANH	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/799,716	DOSHO ET AL.	
	Examiner	Art Unit	
	DINH T. LE	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply.

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 1 is/are allowed.

6)☒ Claim(s) 2-8 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/15/04, 7/1/04 & 11/22/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figures 14, 15A-15B and 16 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections

Claim Rejections - 35 USC § 112

Claims 2–8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction or clarification is required.

In claim 2, it is unclear how the recitation "first voltage" on line 3 and "second voltage" on line 15 is read on the preferred embodiment. Insofar as understood, no such voltages are seen on the drawings. Also, the recitation "the output side" on line 8 lacks clear antecedent basis.

In claim 3, the recitation "the sum" on line 27 lacks clear antecedent basis. It is unclear how the electric currents can be "summed" since no means for performing the summing function is recited in the claim. The same is true for claim 8.

The remaining claims are dependent from the above claims and therefore also considered indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 2 and 8/2 are rejected under 35 USC102 (e) as being anticipated by Hsu (US 2004/0101081A1, S/N=10/065,902).

Hsu discloses in Figures 1 and 4A-4C a filter circuit comprising:

- a first element block having a first capacitive element (C21), one end of the element block being supplied with a first voltage (VCON21);
- a second element block having a voltage buffer circuit (68) which receives a voltage generated at the other end of the first element block and a resistive element (R21) which

is connected in series to the output side of the voltage buffer circuit (68), one end of the second element block being connected to the other end of the first element block; and

- a third element block having a second capacitive element (C22), one end of the third element block being connected to the other end of the second element block, the other end of the third element block being supplied with a second voltage (VCONA21), a first input terminal for receiving a first electric current (KI), the first input terminal being connected to the other end of the first element block; and a second input terminal (I) for receiving a second electric current, the second input terminal being connected to a connection point of the second and third element blocks, the magnitude of the second electric current being N times (1/K) that of the first electric current (where N is a predetermined number), wherein the low-pass filter outputs a voltage generated at a connection point of the second and third element blocks; and

- charge pumps circuit (SWUP21, SWUP22, SWDN21, SWDN22) and an output clock generator (18, Figure 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 6/2 and 7/2 are rejected under 35 USC 103(a) as being unpatentable over Hsu (US 2004/0101081A1, S/N=10/065,902) in view of Ishibashi (US 5,374,904) and further in view of Takasuka et al reference (US 5,150,324).

With regard to claims 6/2 and 7/2, Hsu discloses in Figures 4A-4C a filter circuit comprising all of the limitations of the base claim as stated above but does not disclose that the resistor (R21) is the internal resistor of the voltage buffer (68) and the capacitor (C22) is the MOS transistor. Ishibashi teaches in Figure 1 a PLL circuit comprising the transistors (307-308) being connected to function as the capacitors and Takasuka et al teaches in Figure 4B a switched capacitor circuit (114) functioning as a resistor for being fabricated on an integrated circuit. It would have been obvious to a person having skill in the art at the time the invention was made to employ the transistor as taught by Ishibashi and the switch capacitor circuit as suggested by Takasuka et al in the circuit of Hsu for the purpose of allowing the capacitors and resistors being easily fabricated on the integrated circuit.

With regard to claim 5, it is well known in the art that the voltage buffer such as an operational amplifier has a low output impedance or an internal resistor. A skilled artisan realizes that the resistance value of the resistor (R21) in the circuit of Hsu should be included the output impedance of the voltage buffer (68). Since the resistance value of the resistor (R21) should be selected to accommodate with the required specification of a predetermined system in which the modified circuit of Hsu is to be used., selecting only the output impedance or the internal resistance of the voltage buffer in modified circuit of Hsu is considered to be matter of a design expedient for an engineer. Lacking of showing criticality, it would have been obvious to a person having skill in the art at the time the invention was made to employ only the internal resistance of the voltage buffer of Hsu for the purpose of accommodating with the required specification of the predetermined system.

Allowable Subject Matter

Claims 1, 4/1, 6/1, 6/4 and 8/1 are allowed.

Claims 3, 4/3, 6/3, 7/3, and 8/3 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

The claims are allowed because the prior art does not disclose that the second element block has a resistor being connected in series with a power supply, and a third element block is connected in parallel with the second element block for receiving a second electric current having a magnitude being N times that of the first electric current as combined in claims 1 and 3, and the third element block has a second capacitive element connected to the output side of the second element block for receiving a second electric current having the magnitude being N times that of the first electric current as combined in claim 3. In particular, the power supply (VREF1) in Figure 5B of Hsu is located outside the second element block.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY CALLAHAN can be reached at (571) 272-1740.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DINH T. LE
PRIMARY EXAMINER